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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,120	SAULSBURY ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/21/04* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-16, 18-26 and 28-30* is/are rejected.

7)☒ Claim(s) *8,17 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11/26/04* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 5, "program jump tables hold values, which are offset values from the current program counter value" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States

> before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 7, 9-15, 18, 29, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. (U.S. Patent No. 6,338,160), hereafter referred as Patel et al.

Referring to claim 1, Patel et al. discloses as claimed a very long instruction word (VLIW) processing core (system 20, see Fig. 1, note the whole system 20 comprising JAVA accelerator (detailed structure shown in Fig. 3) is best reasonably and broadly interpreted as a processing unit or core.) comprising: a processing pipeline having N-number of processing paths for processing an instruction comprising N-number of P-bit instructions appended together to form a VLIW, said N-number of processing paths process said N-number of P-bit instructions in parallel on M-bit data words (see Col. 7, lines 32-34, regarding the Patel et al.'s processor is intended to be used with very long instruction word (VLIW) computers; and note the above N, P, and M are variant. Patel et al.'s VLIW is inherently having at least N=2, P=16 or 32; and M=16 or 32 since most computers at year 2000 are at least a 32-bit system); and one or more

register files (such as JAVA registers 44, see Fig. 3) having Q-number of registers (such as JAVA registers 44 having at least Q=2 registers, see Fig. 3), said Q-number of registers being M-bits wide (JAVA registers being such as 16 or 32 bit wide); wherein one of said Q-member of registers in at least one of said one or more register files is a program counter register which stores a current program counter value (JAVA PC, see Col. 4, lines 43-45, regarding the Java registers 44 including the PC, program counter indicating what bytecode is being executed, see also Fig. 3).

As to claims 2, and 11 Patel et al. also discloses: one of said Q number of registers in at least one of said one or more register files is a zero register which always stores zero (this is inherently existing when the registers are initialized or before being used or in the situation when a constant zero value is saved in the register during the execution).

As to claims 3, 12, and 29, Patel et al. also discloses: program jumps are executed by adding a value (such as 2) to the current program counter value (JAVA register PC= A see Col. 7, lines 8-10) stored in the program counter register (JAVA registers 44, see Fig. 3) using a standard add operation (see Col. 7, lines 8-10).

As to claims 4, 13, and 30, Patel et al. also discloses: memory addresses are calculated by adding a value to the current program counter value (JAVA register PC= A see Col. 7, lines 8-10) stored in the program counter register (JAVA registers 44, see Fig. 3) using a standard add operation (see Col. 7, lines 8-10).

As to claims 5, and 14, Patel et al. also discloses, as best understood: program jump tables (see Fig. 9B) hold values, which are offset values from the current program counter value.

As to claims 7, Patel et al. also discloses: said Q-number of registers within each of said one or more register files (JAVA registers 44, see Fig. 3) are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said plurality of register files, said value is propagated to a corresponding global register in the other of said one or more register files, and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said one or more register files (JAVA registers 44, see Fig. 3), said value is not propagated to a corresponding register in the other of said one or more register files. Note if it is interpreted that Patel et al.'s system has only one JAVA register file. Therefore, Q-number of registers

therewithin can be interpreted as private registers. The value written to JAVA registers 44, see Fig. 3, which is a private register within one of said one or more register files, said value is not propagated to a corresponding register in the other of said one or more register files.

As to claims 9, and 18, Patel et al. also discloses: said program counter register (JAVA PC see also Fig. 3) is a global register (note when there is only one register file, the registers therein can also broadly and reasonably be interpreted as a global register).

Note claim 10 comprises the limitations of claim 1 and 7 which are disclosed by Patel et al. as set for the above.

Note claim 15 comprises the limitations of claim 1 which are disclosed by Patel et al. as set for the above.

4. Claims 19, 20, 24, 26, and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Drabenstott et al. (U.S. Patent No. 6,366,999), hereafter referred to as Drabenstott et al.

Referring to claim 19, Drabenstott et al. discloses, as claimed, in a computer system, a scalable computer processing architecture, comprising: one or more processor chips (see

system 20 as shown in Fig. 1), each comprising: a processing core (processing elements: PE1, PE2, and PE3 see Fig. 1), including: a processing pipeline having N-number of processing paths, each of said processing paths for processing instructions on M-bit data words; and one or more register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1), each having Q-number of registers, said Q-number of registers being M-bits wide (note the above N, Q, and M are variant. Drabenstott et al.'s VLIW is inherently having N, Q, and M bit number more than 1), wherein one of said Q-member of registers comprises a program counter register that holds a current program counter value (JAVA PC, see Col. 4, lines 43-45, regarding the Java registers 44 including the PC, program counter indicating what bytecode is being executed, see also Fig. 3); an I/O link (PE local memory & data bus interface, 157, 157', 157', see Fig. 1) configured to communicate with other of said one or more processor chips or with I/O devices (since the processor, as shown in Figs. 1 and 5B, is a VLIW-based processor, see also Col. 6, lines 12-15, regarding "SP/PE0 and the other PEs use a five instruction slot iVLIW architecture which contains a very long instruction word memory (VIM) 109"); a communication controller (cluster switch 171 see Fig. 1, and Col. 6, lines 43-44) in electrical communication with said processing core and said I/O link (PE

local memory & data bus interface, 157, 157', 157', see Fig. 1); said communication controller (cluster switch 171 see Fig. 1, and Col. 6, lines 43-44) for controlling the exchange of data between a first one (such as that comprising PE1) of said one or more processor chips (comprising processing elements: PE1, PE2, and PE3 see Fig. 1) and said other (such as that comprising PE2) of said one or more processor chips (comprising processing elements: PE1, PE2, and PE3 see Fig. 1see Fig. 1); wherein said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said 1/O links (PE local memory & data bus interface, 157, 157', 157', see Fig. 1) of said processor chips, so as to create multiple processing core (processing elements: PE1, PE2, and PE3 see Fig. 1) pipelines which share data therebetween.

As to claim 20, Drabenstott et al. also discloses: one of said Q number of registers in at least one of said one or more register files is a zero register which always stores zero (this is inherently existing when the registers are initialized or before being used).

As to claim 24, Drabenstott et al. also discloses: a processing instruction comprises N-number of P-bit instructions appended together to form a very long instruction word (VLIW)

(as set forth above, since the processor, as shown in Figs. 1 and 5B, is a VLIW-based processor, see also Col. 6, lines 12-15, regarding "SP/PE0 and the other PEs use a five instruction slot iVLIW architecture which contains a very long instruction word memory (VIM) 109"), and said N-number of processing paths process N number of P-bit instructions in parallel (note the above N, P, and M are variant. Drabenstott et al.'s VLIW is inherently having N, P, and M bit number more than 1).

As to claim 26, Drabenstott et al. also discloses: said Q-number of registers within each of said one or more register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1) are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said plurality of register files, said value is propagated to a corresponding global register in the other of said one or more register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1), and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said one or more register files (PE CONFIG REGISTER FILEs, 127, see Fig. 1), said value is not propagated to a corresponding register in the other of said one or more register files. Note the value being propagated to a corresponding global register; and the value being not

propagated to a corresponding private register are inherent for the Drabenstott et al.'s system.

As to claim 28, Drabenstott et al. also discloses: the program counter register is a global register (since the PC value is transferred and commonly used in the Drabenstott et al.'s system).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel et al..

Patel et al. discloses the claimed invention except for explicitly showing that M=64, Q=64, and P=32.

However, it is well known in the art to have a computer system having M=64, Q=64, and P=32.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Patel et al.'s system to comprise M=64, Q=64, and P=32 since it is just an alternative bit size comparing with that used in the Patel et al.'s system.

Further, as shown in re Rose, 105 USPQ 237 (CCPA 1955), to make changes in size/range generally does not provide patentable weight to the claimed invention.

7. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drabenstott et al. in view of Patel et al..

Drabenstott et al. discloses the claimed invention except for: program jumps are executed by adding a value to the current program counter value stored in the program counter register using a standard add operation; memory addresses are calculated by adding a value to the current program counter value stored in the program counter register using a standard add operation; and program jump tables hold values, which are offset values from the current program counter value.

Patel et al. discloses : program jumps are executed by adding a value (such as 2) to the current program counter value (JAVA register PC= A) stored in the program counter register

(JAVA registers 44, see Fig. 1) using a standard add operation (see Col. 7, lines 8-10); memory addresses are calculated by adding a value to the current program counter value (JAVA register PC= A) stored in the program counter register (JAVA registers 44, see Fig. 1) using a standard add operation (see Col. 7, lines 8-10); and program jump tables (see Fig. 9B) hold values, which are offset values from the current program counter value.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Drabenstott et al.'s system to comprise program jumps being executed by adding a value to the current program counter value stored in the program counter register using a standard add operation; memory addresses being calculated by adding a value to the current program counter value stored in the program counter register using a standard add operation; and program jump tables holding values, which are offset values from the current program counter value, as taught by Patel et al., in order to facilitate the operations with program jumps or branches and to facilitate memory addressing for the Drabenstott et al.'s system.

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Drabenstott et al.

Drabenstott et al. discloses the claimed invention except for explicitly showing: using Q=64 registers in the register file.

However, it is well known in the art to have a computer system having Q=64 registers in the register file.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Drabenstott et al.'s system to comprise having Q=64 registers in the register file since it is just an alternative bit size comparing with that used in the Drabenstott et al.'s system.

Further, as shown in re Rose, 105 USPQ 237 (CCPA 1955), to make changes in size/range generally does not provide patentable weight to the claimed invention.

Allowable Subject Matter

9. Claims 8, 17, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Amendment

10. Applicant's arguments filed 7/21/04 have been fully considered but they are not deemed to be persuasive.

Regarding drawings problems, Applicant's response has not completely overcome these objections.

Applicants argue that "Patel has hardware JAVA registers 44 that are outside of CPU 25, Patel. FIG. 3. Those JAVA registers hold the program counter (PC), but those JAVA registers are not within the processing core. … Considering the whole of Patel, it is clear that the PC is not in the register file of the processing core" (page 11, lines 18-23). Examiner realizes the structure of Patel et al.'s system. However, as set forth in the art rejections above, the whole system 20 comprising JAVA accelerator (detailed structure shown in Fig. 3) is best reasonably and broadly interpreted as a processing unit or core. Therefore, the PC is in the register file of the processing core.

Applicants further argue that "one can only presume that Patel (i.e., the present reference, not the parent) does not contemplate the use of VLIW or why would the quoted statement only specify the parent" (page 12, lines 3-5). Examiner disagrees with the Applicants. As clearly indicated in Col. 7, lines 32-34, the Patel et al.'s processor is intended to be used

with very long instruction word (VLIW) computers. A copy of parent, U.S. Patent No. is also cited in this Office Action.

Regarding the argument about zero register in claim 2 (page 12, lines 8-11). Examiner disagrees with the Applicants. As set forth in the art rejections above, Patel et al. also discloses: one of said Q number of registers in at least one of said one or more register files is a zero register which always stores zero (this is inherently existing when the registers are initialized or before being used or in the situation when a constant zero value is saved in the register during the execution). The zero register as claimed is best reasonably and broadly interpreted.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

13. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by

applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

May 16, 2005